REMARKS

Examiner W.D. Coleman is thanked for the thorough examination and search of the subject Patent Application. Claims 10, 15, and 20 have been amended.

All Claims are believed to be in condition for Allowance, and that is so requested.

Reconsideration of the Claims 10 and 15, rejected under 35 U.S.C. 112, first paragraph, is requested based on Amended Claims 10 and 15, and the following remarks.

Claims 10 and 15 have been amended to remove references to "standard" as in the phrase "standard threshold voltage implantation." The term "first" has been substituted.

Reconsideration of the Claims 10 and 15 rejected under 35 U.S.C. 112, first paragraph, is requested Amended Claims 10 and 15, and the above remarks.

Reconsideration of the Claims 15 and 20 rejected under 35 U.S.C. 112, second paragraph, is requested based on Amended Claims 15 and 20, and the following remarks.

The reference in line 21 of original Claim 15 to "said output pin" did appear to have antecedent basis (in line 7). However, Claims 15 and 20 have been amended to correct the use of "mental steps" as described by the Examiner. In addition, Amended Claim 20 changes the reference "said first NMOS" to the correct reference of "said first PMOS."

Reconsideration of the Claims 15 and 20 rejected under 35 U.S.C. 112, second paragraph, is requested based on Amended Claims 15 and 20, and the above remarks.

Reconsideration of Claims 1-24 rejected under 35 U.S.C. 103(a) as unpatentable over Dasse et al (US 5,654,588) in view of Pierrat (US 6,421,111 B1) is requested based on the following remarks.

Applicant agrees that Dasse describes a method/apparatus for wafer-level testing of an integrated circuit device. However, the disclosure of Dasse neither teaches nor suggests

the key elements of Applicant's method, as described by Claims 1-24, such that it would have been obvious to one skilled in the art to practice Applicant's invention.

In particular, Applicant finds that Dasse does disclose the following:

(1) the use of different die designs on one wafer (col. 6, lines 57-63);

(2) mentioning parametric testing to "measure integrated circuit die characteristics over a continuous range of inputs parameters, such as voltage, current, timing, power, etc." (col. 6, lines 5-9);

(3) that each die on the wafer could have a unique code, programmed into nonvolatile cells such as ROM (col. 8, lines 19-26);

(4) that such nonvolatile cells could be programmed by either a ROM programming step (col. 8, lines 36-47) or a programmable light source to define the photoresist (col. 8, lines 48-65) or by a metal conductor layer (col. 15, lines 5-18).

However, Dasse does NOT disclose any of the following:

(1) any method of programming the NV cells involving (1) an additional ion implantation that occurs only when an optional reticle is used in the process, wherein, (2) this ion implantation is made to one transistor in a pair of transistors designed for this purpose;

(2) any method to actually read the programmed transistors. No where does Dasse disclose, hint, or suggest how to read the "unique codes" present on the NV transistors. The mere presence of a reference to "parametric testing" in another section is in no way sufficient to make it obvious to one skilled in the art to use the key teachings of the present invention. Namely, Applicant teaches: (1) setting up two transistors on the same IC where one transistor is either exposed or not exposed to a parameter changing process depending on the use of or non-use of an optional reticle; (2) parametric testing each these two transistors through a testing pin; then (3) comparing the parametric performance of the two transistors; and finally (4) deducing the presence or absence of the reticle option based on this comparison.

The above-described, key features of the present invention

are not disclosed or suggested by Dasse or by Pierrat. It has not been established that it is well-known that ROM cells may be programmed by implanting ions into the cells to alter the threshold voltage. However, even if this is granted, Applicant's unique method of determining the presence/absence of a reticle option is neither well-known, obvious, nor suggested by the cited art.

It is not disclosed, obvious, or suggested in the cited art to force a test voltage through a first MOS transistor drain and gate while measuring the current (Claim 1, lines 3-5), to force the same test voltage through a second MOS transistor drain and gate while measuring the current (Claim 1, lines 11-14), and then to compare the measured currents to detect the presence of absence of a reticle option (Claim 1, lines 19-22). Similarly, performing the measurement of the first and second transistors at an output pin of an integrated circuit (Claim 15, lines 5-7, 14, 18-20, and 28) for the purposed described above is not disclosed, obvious, or suggested by the cited art.

Therefore, because the key features of the present invention are neither disclosed, obvious, or suggested by the cited art, it is requested that the the rejection of Claims 1-

24, as unpatentable over Dasse et al (US 5,654,588) in view of Pierrat (US 6,421,111 B1) be withdrawn.

Reconsideration of Claims 1-24 rejected under 35 U.S.C. 103(a) as unpatentable over Dasse et al (US 5,654,588) in view of Pierrat (US 6,421,111 B1) is requested based on the above remarks.

Applicants have reviewed the prior art made of record and not relied upon and agree with the Examiner that while the references are of general interest, they do not apply to the detailed Claims of the present invention.

Allowance of all Claims is requested.

Attached hereto is a marked-up version of the changes made to the Claims by the current amendment. The attached pages are captioned "VERSION WITH MARKINGS TO SHOW CHANGES MADE."

It is requested that should Examiner W. D. Coleman not find that the Claims are now Allowable that he call the undersigned at 989-894-4392 to overcome any problems preventing allowance.

Respectfully submitted,

Douglas R. Schnabel

Douglas R. Schnabel, Reg. No. 47,927

VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Claims:

Claim 10 has been amended as follows:

10. (AMENDED) A method of detecting a threshold voltage implantation reticle option layer in an integrated circuit device comprising:

measuring the current through a first MOS transistor in an integrated circuit device by forcing a test voltage on the drain and the gate wherein said gate and said drain of said first MOS transistor are connected together, wherein the source of said first MOS transistor is connected to a reference voltage, and wherein said first MOS transistor has [the standard] a first threshold voltage implantation but not [the] a threshold voltage implantation reticle option layer;

measuring the current through a second MOS transistor in said integrated circuit device by forcing same said test voltage on the drain and the gate wherein said gate and said drain of said second MOS transistor are connected together, wherein the source of said second MOS transistor

is connected to a reference voltage, and wherein said second MOS transistor has both said [standard] first threshold voltage implantation and said threshold voltage implantation reticle option layer; and

comparing said current through said first MOS transistor and said current through said second MOS transistor to detect the presence of said threshold voltage implantation reticle option layer in said integrated circuit device.

Claim 15 has been amended as follows:

15. (AMENDED) A method of detecting a threshold voltage implantation reticle option layer in an integrated circuit device comprising:

selecting a first NMOS transistor in an integrated circuit device in a first test mode [so that] to couple the voltage at the drain and the gate of said first NMOS transistor [may be measured at] to an output pin of said integrated circuit device wherein said gate and said drain of said first NMOS transistor are connected together, wherein the source of said first NMOS transistor is connected to ground, and wherein said first NMOS transistor

has [the standard] a first threshold voltage implantation but not [the] a threshold voltage implantation reticle option layer;

measuring said voltage at said output pin in said first test mode when an internal [standard] test voltage is connected to said drain and said gate of said first NMOS transistor through a first internal standard resistance;

selecting a second NMOS transistor in said integrated circuit device in a second test mode [so that] to couple the voltage at the drain and the gate of said second NMOS transistor [may be measured at] to said output pin of said integrated circuit device wherein said gate and said drain of said second NMOS transistor are connected together, wherein the source of said NMOS transistor is connected to ground, and wherein said second NMOS transistor has both said [standard] first threshold voltage implantation and said threshold voltage implantation reticle option layer;

measuring said voltage at said output pin in said second test mode when said internal [standard] test voltage is connected to said drain and said gate of said second NMOS transistor through a second internal standard resistance; and

comparing said voltage at said output pin in said

first test mode with said voltage at said output pin in said second test mode to detect the presence of said threshold voltage implantation reticle option layer in said integrated circuit device.

Claim 20 has been amended as follows:

20. (AMENDED) A method of detecting a threshold voltage implantation reticle option layer in an integrated circuit device comprising:

selecting a first PMOS transistor in an integrated circuit device in a first test mode [so that] to couple the voltage at the drain and the gate of said first PMOS transistor [may be measured at] to an output pin of said integrated circuit device wherein said gate and said drain of said first [NMOS] PMOS transistor are connected together, wherein the source of said first PMOS transistor is connected to an internal standard voltage, and wherein said first PMOS transistor has the standard threshold voltage implantation but not the threshold voltage implantation reticle option layer;

measuring said voltage at said output pin in said

first test mode when said drain and said gate of said first PMOS transistor are connected to ground through a first internal standard resistance;

selecting a second PMOS transistor in said integrated circuit device in a second test mode [so that] to couple the voltage at the drain and the gate of said second PMOS transistor [may be measured at] to said output pin of said integrated circuit device wherein said gate and said drain of said second PMOS transistor are connected together, wherein the source of said second PMOS transistor is connected to said internal standard voltage, and wherein said second PMOS transistor has both said standard threshold voltage implantation and said threshold voltage implantation reticle option layer;

measuring said voltage at said output pin in said second test mode when said drain and said gate of said second PMOS transistor are connected to said ground through a second internal standard resistance; and

comparing said voltage at said output pin in said first test mode with said voltage at said output pin in said second test mode to detect the presence of said threshold voltage implantation reticle option layer in said integrated circuit device.